REMARKS/ARGUMENTS

Specification

The Examiner objected to the specification stating that items were listed as "XXX" and "YYY" at page 1 line 10. Applicant respectfully requests the Examiner to withdraw this objection in view of a preliminary amendment that was filed on February 21, 2001. Specifically, at the top of page 2 of this amendment, Applicant had replaced XXX with 20 and YYY with 1,917.

The Examiner also objected to the specification for containing website addresses, e.g. at page 4 of the specification. Applicant respectfully requests the Examiner to withdraw this objection because the web addresses are **not** being used to incorporate by reference the external subject matter in support of the invention description. Instead, these web addresses are provided in the Background section, simply to identify sources of information available on the Internet. To the extent the Examiner objects to these addresses as being browser executable hyperlinks, the specification is amended as shown above to change their format.

Accordingly, reconsideration and withdrawal of all specification objection is respectfully requested.

Claim Rejections – 35 U.S.C. §102

Claim 1 was rejected under 35 U.S.C. §102(b) as being anticipated by an article entitled "Partitioned ROBDDs – A Compact, Canonical and Efficiently Manipulable Representation for Boolean Functions" by Amit Narayan et al, ICCAD '96. In explaining the rejection, the Examiner stated that Narayan's section 4.1 provides for reading of data corresponding to variables f and g, that the second paragraph of section 3.2.1 indicates the data, and the Examiner further stated that Narayan inherently solves various cad problems and reduces space requirements for ROBDDs (as per paragraphs 2 and 3 of section 1).

Assuming that the Examiner is correct in their characterization of Narayan's teachings, the Examiner's statements at most teach that the names in "two circuits f and g" are to be replaced. Note that it is circuits f and g whose satisfiability is being checked by Narayan.

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In contrast, Claim 1 requires that name replacement be done on circuit elements against which satisfiability is to be checked. This is because Claim 1 states that the first data (on which name replacement is being done) corresponds to **a first cell of ... a library used in manufacturing said integrated circuit.** (emphasis added). Narayan provides no indication whatsoever that a library cell's names are to be replaced.

In view of the above remarks, Applicant submits that the Examiner has failed to make a prima facie case of rejection of Claim 1. To the extent the Examiner relies on inherency to state that circuits f and g represent circuit elements in a cell library, the Examiner is respectfully requested to identify a specific location (by page and line number in the Narayan article) from which this necessarily follows. In this context, Applicant respectfully draws the Examiner's attention to the evidentiary requirement to be met: "If Applicant Challenges a Factual Assertion as Not Properly Officially Noticed or not Properly Based Upon Common Knowledge, the Examiner Must Support the Finding With Adequate Evidence." See MPEP 2144.03. If the Examiner is unable to find an appropriate citation then Claim 1 must be allowed.

Claims 2-14 depend from Claim 1 and are therefore believed to be patentable for at least the same reasons as those discussed above for Claim 1. The remaining Claims 15-23 are also believed to be patentable for one or more reasons similar to those discussed above.

Claim Rejections – 35 U.S.C. §103

Claim 5 was rejected by the Examiner as being obvious over the teachings of Narayan, with the Examiner explaining the rejection as follows: "The order of replacing names is considered a choice of design; since, the overall functionality remains the same in that one name is merely replaced with another."

Applicant submits that the Examiner appears to have a fundamental misunderstanding of the Applicant's invention as recited in Claim 5. It is not a design choice to obtain a first renamed data and to also obtain a second renamed data, because **multiple renamed data** are obtained, albeit by changing the order of replacement. Even if the Examiner is correct in stating that it is a design choice to prepare second renamed

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data instead of first renamed data, there is no suggestion whatsoever that multiple renamed data are to be prepared.

When multiple renamed data are prepared as per Claim 5, matching occurs implicitly, regardless of the order in which the names occur in the original cell and in the original circuitry. In this context, Applicant respectfully draws the Examiner's attention to the following paragraph at page 6 line 26 to page 7 line 2:

> In case of asymmetric cells, a number of cell models are built in one embodiment using different orders of names, to ensure that at least one of these cell models matches a circuit model (as the order of names of signals input to a circuit model depend on remaining portions of the electrical circuit). Therefore, a single asymmetric cell is related (as described above) to a number of models that differ only in the order of the input signals and/or inversion of one or more input signals. Use of multiple cell models for a single cell allows matching to occur implicitly when modeling portions of the circuitry, regardless of the order in which the names occur in the original cell and in the original circuitry.

In view of the above, Applicant respectfully requests the Examiner to withdraw the obviousness rejection of Claim 5. If the Examiner continues to reject Claim 5 as being a design choice over Narayan's disclosure, Applicant respectfully requests the Examiner to provide a prior art citation for the motivation to prepare multiple renamed data.

Claim 6 was rejected for the same reasons as Claim 1, without providing any further detail. Specifically, the Examiner has not provided any citation whatsoever for the acts of "relating" recited at the end of Claim 6. For this reason, Applicant respectfully submits that the Examiner has failed to make a prima facie case of rejection of Claim 6.

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Moreover, despite the Examiner's statement that the features of Claim 6 are taught by the plurality of data as per the rejection of Claim 1, Applicant submits that there is no

indication whatsoever in Narayan that **renamed data is used in generating at least two ROBDD models**.

For the above reasons, Applicant respectfully requests allowance of all pending Claims 1-23. Should the Examiner have any questions concerning this response, the Examiner is invited to call the undersigned at (408) 982-8200, ext. 3.

Via Express Mail Label No.
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Respectfully submitted,

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